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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,111	10/22/2003	Richard C. Foss	2037.1003-013	5335

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EXAMINER	
NGUYEN, HIEN N	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,111	FOSS, RICHARD C.	
	Examiner	Art Unit	
	Hien N. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the Amendment filed on 11/22/04*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search report*.

DETAILED ACTION

The amendment filed on 11/22/04 ahs been entered.

Claims 1-4 have been canceled.

Claims 5-25 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 5-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Tran (U.S Patent No 5,638,317).

With respect to claim 5, figure 3b of Tran discloses a memory device comprising a plural of storage cells (120), at least one secondary data buses (MAIN I/O) that is centrally located between the plural arrays (between the array 120 in the left side and

the other array in the right side of figure 3b), extending in a first direction (namely vertical direction), a plurality of primary data buses (LOCAL I/O) coupled to the second data buses (the local data bus is selectively connected to the main data bus by transistor 146), each of the plurality of the primary data buses coupled to one of the array (the local I/O is connected to the cell array as shown in figure 3b), and the primary data buses is extended in a second direction (namely horizontal direction) orthogonal to the first direction (vertical).

With respect to claim 6, each primary data bus (LOCAL I/O) is coupled to a bit line sense amplifier (S/A figure 3b) and each bit line (the line inside the cell array 120; note that every memory cell array must have a plurality of bit lines and a plurality of word lines so as select address and data in any operation of the memory device) being parallel to the primary data bus LOCAL I/O.

With respect to claim 7, the sense amplifier of Tram clearly senses the data to full logic.

With respect to claim 8, the circuit of Tran is used for driving a DRAM (see column 5, lines 20-25).

With respect to claim 9, the cell array 120 is mirror with the array in the right side of figure 3b.

With respect to claim 10, the local differential amplifier (LOCAL DIFF AMP) would be considered as a data buses sense amplifier that is coupled between the primary and secondary data buses.

With respect to claim 11, the transistor 146 would be an isolation device between the data buses sense amplifier and the secondary data buses, because this transistor performs the function of connecting or disconnecting the data bus sense amplifier and the secondary data buses.

With respect to claim 12, the transistor 130 would perform the function of selectively coupled the data bus sense amplifier (LOCAL DIFF AMP) to the primary data bus (LOCAL I/O).

With respect to claims 13 and 14, since the memory device of Tran has multiple specific applications, then the circuit of Tran would meet the claimed limitation as claimed in this claim.

With respect to claim 15, figure 3B shows both mirror arrays are addressed by the YDEC decoder to control which data bus to be accessed at a particular time (time shared limitation).

With respect to claim 16, the two secondary data buses (MAIN I/O) include two parallel data buses.

With respect to claim 17, Tran discloses a memory device comprising plural memory arrays (figure 5, A array, B array), a pair of bit lines (BL1B, BL2B, fig.5), each bit line pair corresponding to a sense amplifier (SA, figure 5), word lines (WLn, WLn+1, figure 5) crossing the bit lines, storage cell (cell 1B, cell 2B, cell 1A, cell 2A, figure 5), pairs of primary data buses (LOCAL I/O, figure 3b) parallel (in a horizontal direction) to the bit lines (BL1B, BL2B, figure 5) coupled to a bit line sense amplifier (S/A, figure 3b) through first access device (14, figure 3b), pair of secondary data buses (MAIN I/O)

orthogonal to the primary data buses (LOCAL I/O), centrally located between plural arrays (120 and the array in the right side).

With respect to claim 18, the applicant is referred to the rejection applied to claim 6 for the reasons of this rejection.

With respect to claim 19, the cell in the array 120 is clearly a storage cell.

With respect to claim 20, the applicant is referred to the rejection applied to claim 9 for the reasons of this rejection.

With respect to claims 21 and 22, the applicant is referred to the rejection applied to claims 13 and 14 for the reasons of this rejection.

With respect to claim 23, the step of selectively enabling charge storage cells is performed by the decoder (YDEC, figure 3b), the step of sensing stored charge is performed by the sense amplifier S/A (figure 3b), the step of coupling bit line sense amplifier to the primary data bus is performed by transistor 14 (figure 3b), and the step of coupling the primary data buses to the secondary data buses is performed by transistor 146 (figure 3B).

With respect to claim 24, the step of coupling each pair of primary data buses (LOCAL I/O) is performed by transistor 130 (figure 3B).

With respect to claim 25, the applicant is referred to the rejection applied to claim 7 for the reasons of this rejection.

Response to Arguments

Applicant's arguments with respect to claims 5-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Foss (6,661,723) and Miyano et al.(6,154,406) are cited as of interest.

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hien N. Nguyen whose telephone number is (571) 272-1879. The examiner can normally be reached on Monday through Thursday 9:30 AM to 7:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen
February 18, 2005

ANH PHUNG
PRIMARY EXAMINER